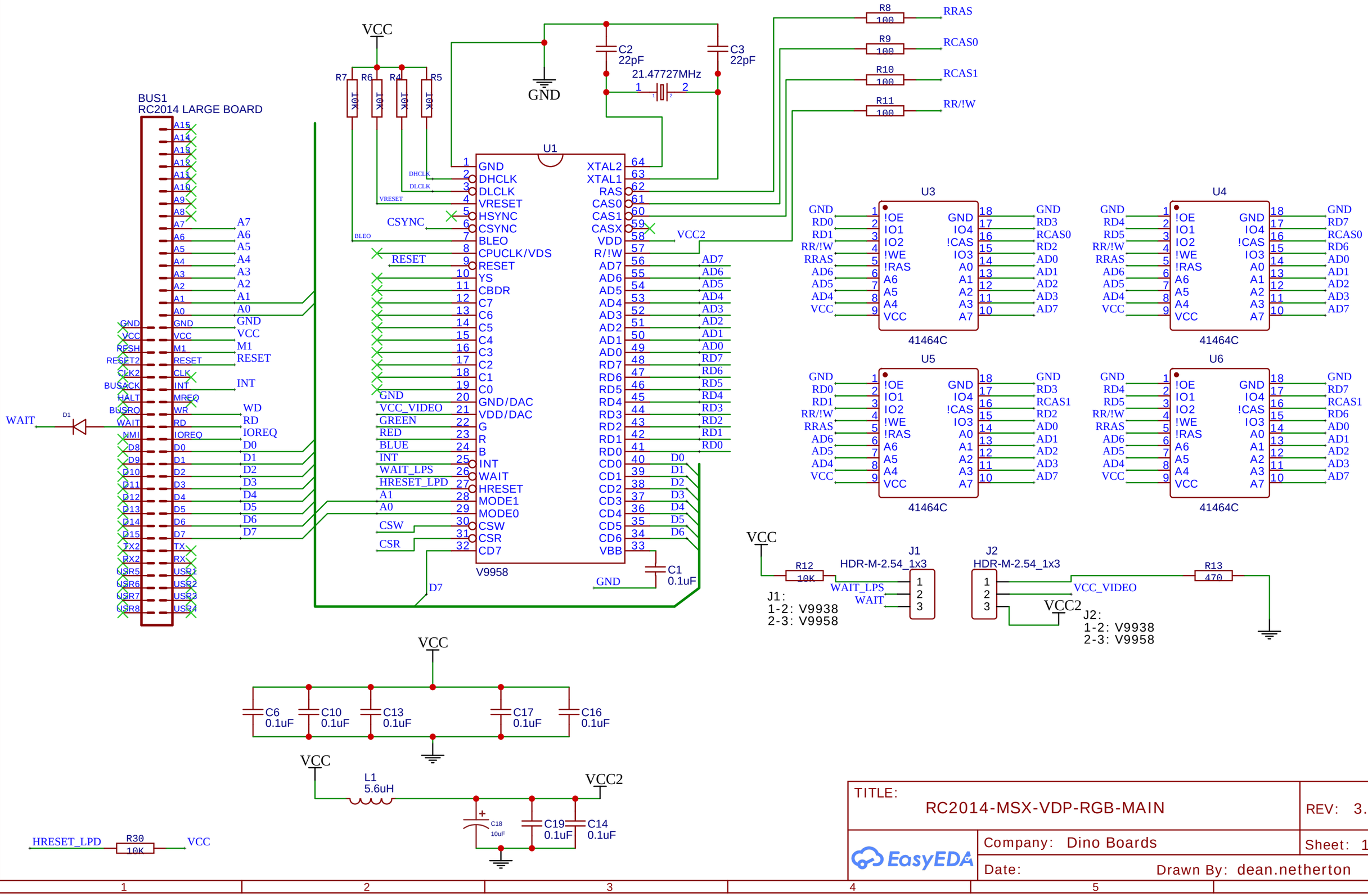
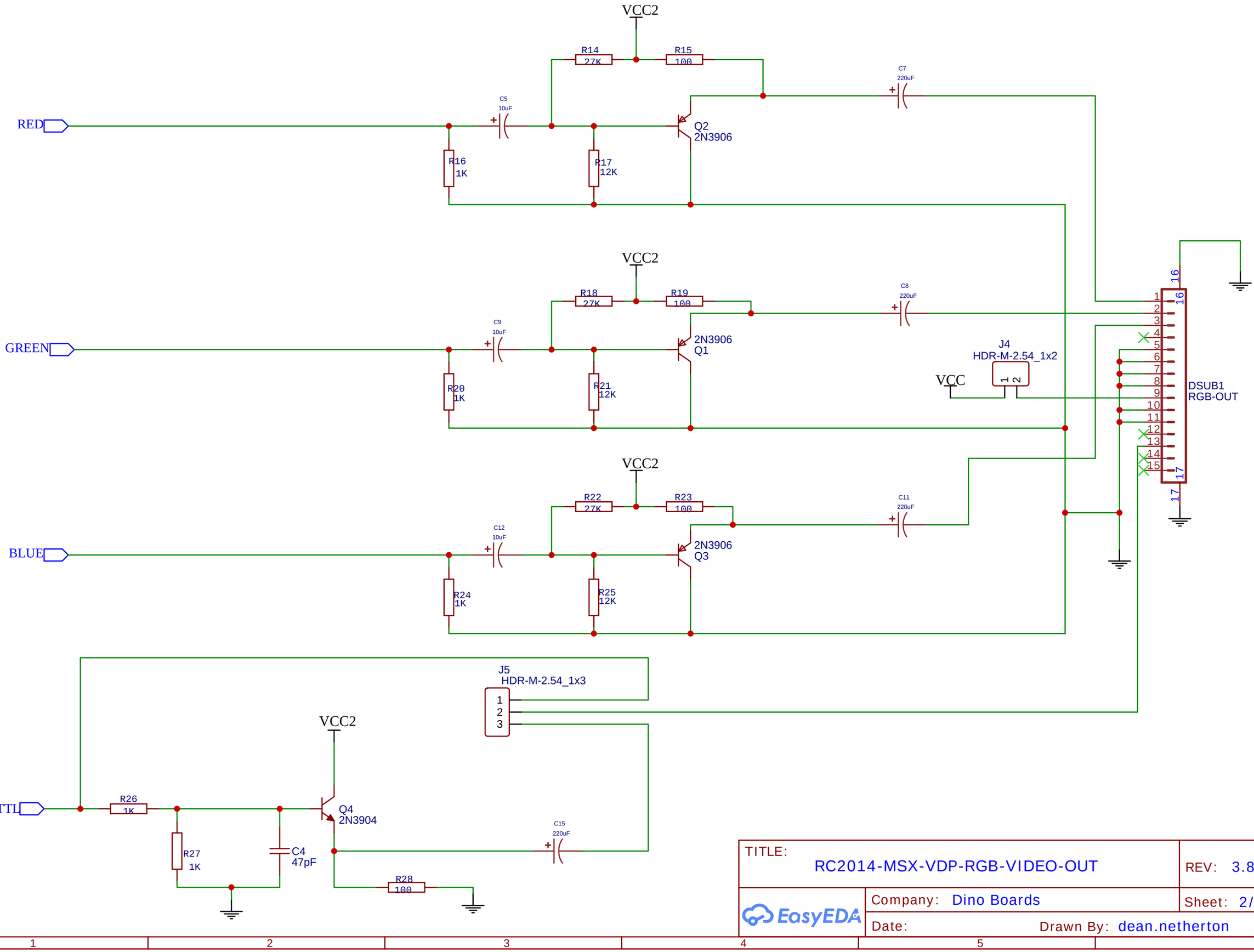
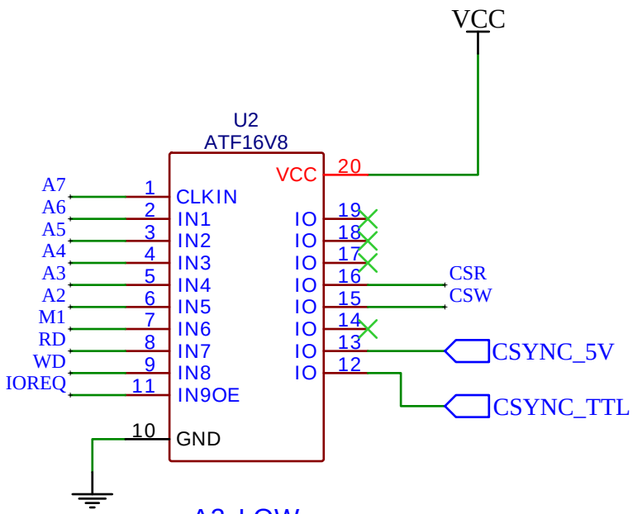


TITLE: RC2014-MSX-VDP-RGB-MAIN			REV: 3.8
EasyEDA	Company: Dino Boards		Sheet: 1/4
	Date:	Drawn By: dean.netherton	



TITLE: RC2014-MSX-VDP-RGB-VIDEO-OUT		REV: 3.8
EasyEDA	Company: Dino Boards	Sheet: 2/4
	Date:	Drawn By: dean.netherton



A2-LOW
A3-HIGH
A4-HIGH
A5-LOW
A6-LOW
A7-HIGH
IOREQ-LOW

$98->9B

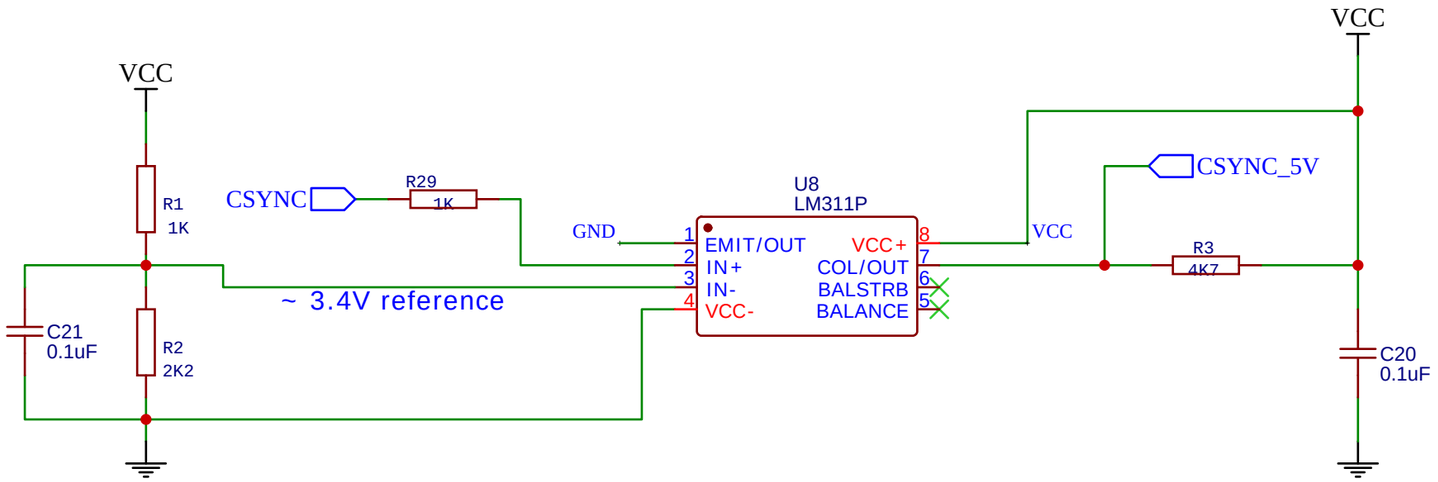
PLD Code

```
Name     v9958-cs-v3.8-and-up;
PartNo   00 ;
Date     15/12/2020 ;
Revision 01 ;
Designer Dean Netherton ;
Company  Dino ;
Assembly None ;
Location Ignored ;
Device   g16v8a ;


/************* INPUT PINS *********************/
PIN  1 = A7;
PIN  2 = A6;
PIN  3 = A5;
PIN  4 = A4;
PIN  5 = A3;
PIN  6 = A2;
PIN  7 = !M1;
PIN  8 = !RD;
PIN  9 = !WR;
PIN 10 = GND;
PIN 11 = !IORQ;

/*************** OUTPUT PINS *********************/
PIN 12 = CSYNC_TTL;
PIN 13 = CSYNC_5V;
//PIN 14 = NC;
PIN 15 = !CSW;
PIN 16 = !CSR;
//PIN 17 = NC;
//PIN 18 = NC;
//PIN 19 = NC;
PIN 20 = VCC;

CSYNC_TTL = CSYNC_5V;

ADDR = A7 & !A6 & !A5 & A4 & A3 & !A2;   // $98 TO $9B
CS = ADDR & IORQ & !M1;

CSW = CS & WR;
CSR = CS & RD;
```

TITLE: RC2014-MSX-VDP-RGB-ADDR-DECODING		REV: 3.8
EasyEDA	Company: Dino Boards	Sheet: 3/4
	Date:	Drawn By: dean.netherton

V9938/58 - CSYNC

V9958 - CYSNC 3V to 5V
V9938 - CSYNC 2.7V to 3.7V



TITLE: RC2014-MSX-VDP-RGB-CSYNC		REV: 3.8
EasyEDA	Company: Dino Boards	Sheet: 4/4
	Date: 2024-06-12 Drawn By: Dean Netherton	